High-Performance VLSI Designs Using Pegasus for Efficient IR Drop Reduction

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Abstract *The trend of shrinking technology nodes has resulted in more cells being densely packed into smaller areas, which has led to a substantial increase in peak current demands. This, in turn, has created regions with high current requirements that can lead to IR drop hotspots, adversely affecting cell speed and overall chip performance. Therefore, it is crucial to mitigate IR drop, and we propose a solution that involves adding smart power and ground metal fills after the Place-and-Route (PNR) process. This approach can improve IR drop without compromising the device's timing. The IR drop issue in VLSI designs has become critical in determining performance and reliability. The Power/Ground (P/G) network, more especially the Power Distribution Network (PDN), is where IR drop usually happens. It can lead to signal nets, especially clock nets, performing poorly. As interconnects are scaled down aggressively, the width of the wires decreases, leading to an increase in the interconnects' resistance and inductance (R/L). The higher resistance exacerbates IR drop across the interconnects, leading to a lower voltage being delivered to the cells within the design. This voltage drop significantly impacts the speed and overall functionality of the design. As technology scales down, the supply voltage also decreases, intensifying the impact of IR drop. The change in the output relative to the input of CMOS gates and their noise margins are significantly affected when the ratio of voltage drop to the ideal supply voltage increases. If the IR drop in the P/G network is excessive, it can cause failures in dynamic logic and lead to timing violations in static logic. Designing an effective power grid to accommodate higher current demands due to increased cell density and clocking frequency has become more challenging with the shrinking of technology nodes (such as N16 and N7). In this context, we address the challenges of power grid architecture while maintaining efficient resource routing in the latest technology nodes. Additionally, we explore advanced techniques like timing-aware smart fill technology, which enhances both static and dynamic IR drops while reducing the effective resistance of the power grid.*

Keywords: — IR drop, Power Distribution Network (PDN), VLSI, Pegasus

I. INTRODUCTION

IR drop refers to the voltage reduction in the metal wires of a power grid before it reaches the power pins of standard cells. Limiting IR drop is crucial because it affects the chip's speed and overall performance. It is crucial to conduct comprehensive testing to guarantee the power grid's resilience to various operating conditions, including noise in the Power Distribution Network (PDN). The IR drop problem is becoming more and more important in VLSI designs because it can negatively impact signal nets, particularly clock nets. Wire widths fall as interconnects are aggressively scaled, increasing inductance and resistance. This may have a major effect on the design's functionality and speed. As technology nodes shrink, the impact of IR drop becomes more severe, as supply voltages also

decrease. The change in output with respect to input in CMOS gates and their noise margins are greatly affected when the voltage drop relative to the optimal supply voltage increases. Furthermore, a high drop in the PDN can cause dynamic logic to fail and static logic to encounter timing violations.

As we advance to smaller technology nodes in IC and chip design, wires become thinner along with transistors. This leads to increased wire resistance, which becomes a dominant factor in technology nodes of 16nm and below.

1.1 Motivation for the present work

Several challenges arise as technological nodes shrink to meet the demand for higher package density and enhanced functionality in VLSI (Very Large Scale Integration) chips. This trend leads to lower supply voltages, and the increasing number of cells within a chip necessitates more connection nets. With the power supply scaling alongside the MOSFET size and the extended power supply grid within the chip adding more resistance, it becomes crucial to conduct IR drop analysis. This analysis ensures that each cell in the design receives the necessary voltage for optimal performance.

In chip design, IR drop (voltage drop) occurs due to the Power Distribution Network (PDN) resistance that supplies power to the various components. Maintaining proper IR drop levels is essential to ensure the stable and reliable operation of the chip. Therefore, maintaining proper IR drop is critical in ensuring the stable and reliable operation of the chip. This can be achieved through careful design and optimization of the PDN. So IR Drop is one of the critical issues in chip designing at signoff stage.

II. LITERATURE REVIEW

Sushant Saurabh et al.[1]: With advancements in technology, challenges related to power, area, and timing have become more significant. As technology scales down, the density of cells in a given area increases, leading to a substantial rise in peak current demands.

Yue-Hui Huang et al. [2]: This article discusses the IR drop in multilayer PCBs and presents a study that simplifies the analysis using an adaptive mesh. The study reveals that the VRM's vias contact and copper planes significantly contribute to IR drop.

Amareshwar Marni et al. [3]: This article examines IR voltage drop in nanometer technology, highlighting the limited tools available to address it. The authors propose a new feature in Redhawk that simplifies and automates the resolution of EM and IR voltage drop issues.

Shreyasi Ghosh Dastidar et al. [4]: This article explores how the self-heating effect in electronic devices generates more heat in structures, impacting interconnect reliability. The study uses the Redhawk Tool to analyze a chip design provided by STMicroelectronics, assessing temperature changes across different metal layers and the impact of self-heating. The paper suggests using decoupling capacitors to reduce power consumption in the design. It highlights the importance of considering delta T modeling, which was not previously included in the design process.

III. METHODOLOGY

The increasing significance of VLSI (Very Large-Scale Integration) system performance and reliability has made the "IR drop" phenomenon a critical concern. IR drop occurs primarily in the power/ground network of VLSI designs and can lead to signal net issues, particularly with clock nets. This problem in the power distribution network (PDN) arises when interconnects are aggressively scaled, resulting in narrower interconnects and increased resistance and inductance (R/L) of the wires. This drop can significantly impact the design's speed and functionality. A significant drop in the PDN can cause timing errors in static logic and even failure in dynamic logic.

IR drop analysis can be divided into two categories based on how current is calculated from total power, and the choice of analysis type depends on this calculation. These two types of IR drop analysis are

-Static IR Drop Analysis

- Dynamic IR Drop Analysis

3.1 IR drop Calculation

In the context of IR drop analysis, the ohms' law formula V = IR is used to calculate the voltage drop (V) across a wire, given the current flowing through it (I) and the resistance of the wire (R). The goal is to ensure that the voltage at each node in the circuit is above a certain threshold, typically specified by the circuit's timing and reliability requirements. To compute the current value Total Power P, first calculate the power (Total power) and then use the formula to determine the current.

$$P = V * I \qquad \text{....(i)}$$

When transistor switching activity is strong, the voltage drops, a phenomenon known as dynamic IR drop. The switching time of the logic determines it, while the clock period has less of an impact. The formula for dynamic IR drop is

$$Vs = I_{avg} \times R_{wire}$$

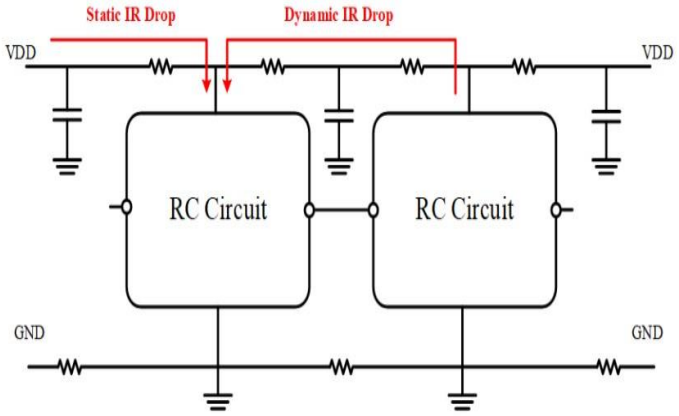

Fig. 1: IR drop in ASIC Design

IV. Proposed PEGASUS Flow

As technology nodes shrink, the resistance (R) and inductance (L) of the power grid (pg) increase, leading to higher static and dynamic IR drops. These issues can cause timing violations and degrade performance. Innovative techniques like "smart fill" are employed to address these challenges. This technique involves adding extra metal structures (fill structures) in unused areas of the chip layout to lower the pg's resistance and inductance. The placement and density of these fill structures are optimized to reduce voltage drops without impacting the timing of the design. The increased power dissipation per unit area results in localized heating and the risk of thermal runaway. To mitigate these issues, designers must manage power distribution carefully, strategically place power-intensive blocks, and use power gating techniques to reduce overall power consumption. As transistor counts rise, the complexity of the power network also increases, posing further challenges in power integrity verification and optimization.

4.1 PG Fills ECO Flow

The flow chart for backend chip design begins with floor planning and power planning. During the **floor plan** stage, the chip's functional blocks are strategically arranged to optimize the chip's size and interconnect routing, while meeting performance and power targets.

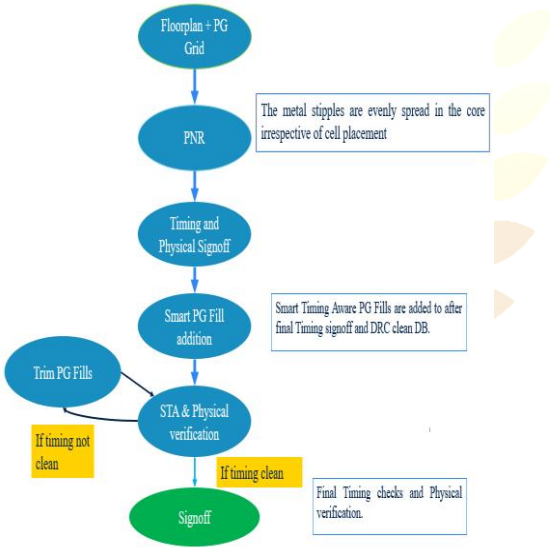

Fig. 2: Flow chart depicting ECO PG fills

This stage also defines the chip's power domains, which sets the stage for the subsequent power planning.

V.RESULTS AND DISCUSSIONS

Reinforcing the power grid (PG) in chip design entails a variety of techniques to ensure uniform power distribution and lower voltage drop across the chip. These methods include utilizing thicker metal wires, expanding

the power rails, adding more metal layers to the PG, and installing decoupling capacitors in strategic locations to lessen infrared drop. These measures collectively enhance the robustness and efficiency of the power grid, ensuring reliable operation of the chip. Furthermore, simulations and tests are conducted to assess the performance and stability of the PG design, allowing for iterative improvements.

Implementing intelligent power-ground metal fills in the PG grid results in a more efficient current distribution throughout the design. Tables 1 and 2 below illustrate the impact of Power Ground fills on instance counts across different blocks, with and without PG fills. The difference is significant. For Block_1, the number of instances experiencing a voltage drop of 100-150 millivolts has decreased by 42.7% compared to the previous value. Similarly, for Block_2, the decrease is 50.2%, and for Block_3, it is now 37.6% of the previous value.

TABLE 1. Vless dynamic drop before PG Fills

Blocks	**Before Power Ground Fill**		
	Greater than150	100 to 150mV	50 to 100mV
Block_1	0	6870	1131833
Block_2	39	35189	1159503
Block_3	29	55070	4207388

TABLE 2: V Less Dynamic Drop after PG Fills

When STA done data is taken into account for power noise analysis, the resulting IR map is shown in Fig. 3, with red dots indicating large voltage drops in certain parts of the chip.

Blk	**After Power Ground Fill**		
	Greater than 150	100 to 150mV	50 to 100mV
Block_1	0	3929	939318
Block_2	7	17531	875330
Block_3	8	34290	3229656

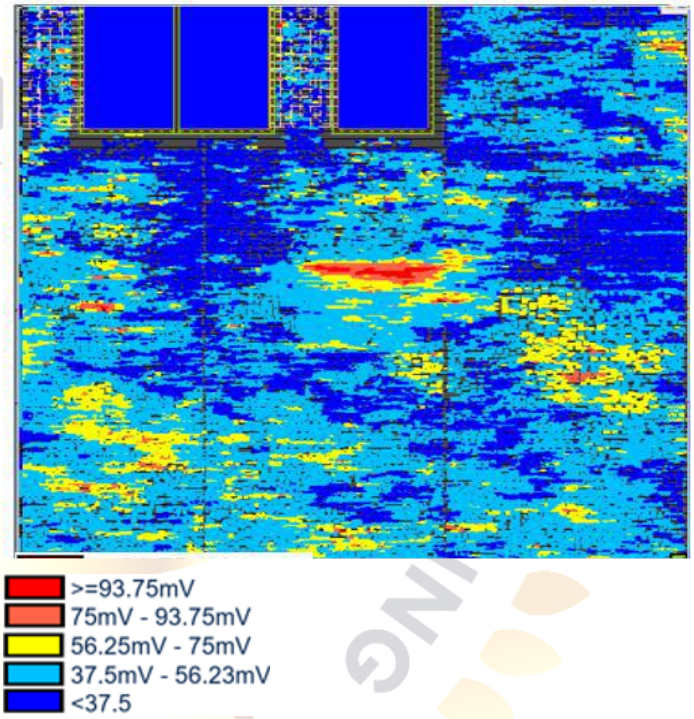

Figure 3 Drop map before Power Ground fills

The orange, yellow, and sky-blue spots all exhibit drops in the range of 75mV-93.75mV, 56.25mV-75mV, and 37.5mV-56.23mV, respectively, while the red spots show drops over or equal to 93.75%. Dark blue, on the other hand, exhibits a decrease below 37.5 mV.

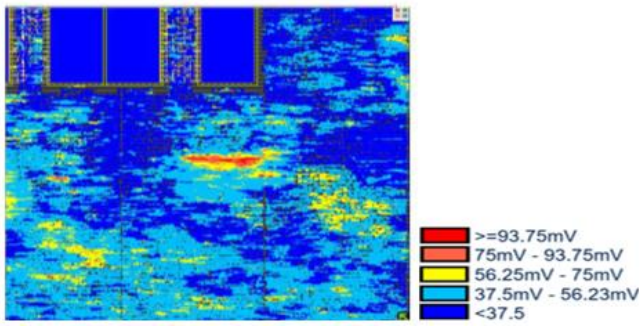

Fig. 4. Drop map after Power Ground fills

Adding PG fills with Pegasus considerably decreased the occurrences with larger voltage drop, as illustrated in Fig. 3.

Fig 4. displays a comparison between the instance count that experienced more drop with and without Power Ground fills. Implementing this technique has proven highly effective in reducing dynamic and overall static IR drop within the design, simplifying the IR-based signoff process. By incorporating smart fills, the design meets its timing requirements, maintains control over

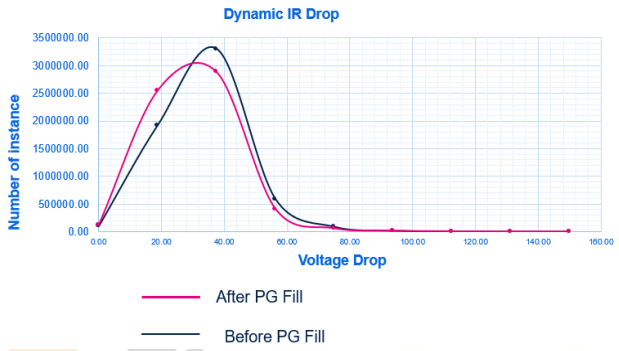

Fig. 5: Instance count Vs drop with and without PG fills.

VI. CONCLUSION

Physical Design Rule Checks (DRCs), and prevents the introduction of new Antenna violations. This method is particularly beneficial for lower technology nodes and complex designs, where it has demonstrated significant advantages in optimizing design runtime and ensuring on-time delivery. The integration of this approach with the Pegasus flow has further streamlined the design process, contributing to more efficient project timelines and higher overall productivity.

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